Electrochemical Nanostructuring of *n*-GaAs Photoelectrodes

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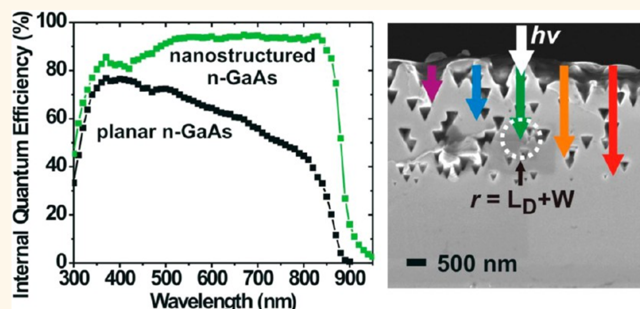
ABSTRACT Methods to simultaneously optimize carrier collection and light in-coupling in semiconductors are important for developing low-cost, high-efficiency photovoltaics and photoelectrodes. We anodically etched nanostructures into planar ⟨100⟩ *n*-GaAs wafers with different bulk minority carrier diffusion lengths L_D. The structures were varied by changing the anodization parameters. A ferrocene/ferrocenium electrolyte provided a conformal rectifying contact to the anodized *n*-GaAs and enabled the measurement of carrier generation and collection as a function of nanostructure geometry and L_D. Internal quantum efficiency Φ_{int} of photoelectrodes varied with nanostructure geometry and L_D. External quantum efficiency Φ_{ext} also depended on the reflectance of the nanostructured GaAs—electrolyte interface. Reflectance was minimized using anodization current densities of 100—150 mA cm^{-2}, which etched subwavelength trigonal prismatic nanostructures ~400 nm in width at their base. For Si-doped *n*-GaAs with L_D = 170 nm, peak Φ_{ext} of ~75% and Φ_{int} of ~85% was achieved using J_{anod} = 150 mA cm^{-2}. The control of both surface nanostructure (to minimize reflection) and pore depth and spacing (to optimize 3D carrier collection) *via* two-step anodization yielded photoelectrodes with peak Φ_{ext} of ~85% and peak Φ_{int} of ~95% for Te-doped *n*-GaAs with a bulk L_D of only 420 nm. The measured short-circuit current densities for the nanostructured photoelectrodes were up to 2.5 times that of planar controls, demonstrating that appropriate nanostructuring significantly improves carrier collection even for direct bandgap materials with large absorption coefficients like GaAs.



KEYWORDS: solar energy · electrochemistry · photoelectrode · GaAs · nanostructure · patterning · anodization

Understanding the interplay between nanostructure, optical reflectance (*R*), and carrier collection is important for the design of photoelectrochemical (PEC) and photovoltaic (PV) devices.[1−3] The ideal structure minimizes both light reflection at the surface and electron—hole recombination in the bulk.[4,5] Bulk recombination occurs when light is absorbed in the semiconductor at a depth greater than the collection length, given by the bulk minority carrier diffusion length L_D plus the depletion width *W*; that is, $L_D + W$ (Figure 1A). One method to reduce bulk recombination is to increase L_D by using a material pure and free of defects, which contributes to the cost of the final device. For PV devices, *R* is reduced by antireflective coatings with optimized thicknesses and indices of refraction (*n*). For PEC applications, the requirement of direct solution—semiconductor contact precludes the use of such coatings (Supporting Information, Figure S1). Therefore, architectures which maximize optical in-coupling from low-*n* (solution or air) to high-*n* (semiconductor) media while simultaneously minimizing bulk recombination losses, and can be implemented without adding expensive or slow processing steps, are needed.

Three-dimensional (3D) structuring provides a mechanism to minimize *R*. For example, arrays of nanoscale cones and pillars nearly eliminate reflection from Si films.[3] This is caused by a gradient in the effective *n* at the air-semiconductor interface due to the subwavelength (λ) size and tapered nanostructure shape.[3] In the Si PV industry an anisotropic wet etching of crystalline Si is used to provide pyramidal surface textures which reduce the *R* value of commercial PV devices.[6,7]

Enhanced carrier collection in 3D radial-junction PV devices relative to planar ones has been modeled by Kayes *et al.*[4] The optical absorption coefficient α(λ) determines the depth to which photons are absorbed in the semiconductor, ∝ α(λ)$^{-1}$.

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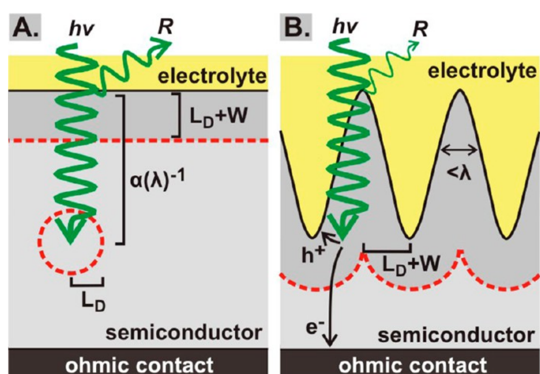


Figure 1. (A) In a planar photoelectrode significant bulk recombination losses occur when light is absorbed at a depth greater than $L_D + W$. (B) Lateral carrier collection in a nanostructured photoelectrode enables collection of minority holes that would otherwise recombine. Surface features with sub-λ dimensions also decrease R losses.

When $L_D + W < \alpha(\lambda)^{-1}$, significant recombination losses occur (Figure 1). The optimal height and spacing of the nanostructures are thus expected to depend on both $\alpha(\lambda)$ and $L_D + W$.[4] When $L_D + W \gg \alpha(\lambda)^{-1}$, bulk recombination does not significantly affect the internal quantum efficiency (Φ_{int}). When $L_D + W < \alpha(\lambda)^{-1}$ (as is typical in many low-cost semiconductors) the 3D structure has a large effect on Φ_{int}.[8] Because $\alpha(\lambda)$ decreases as the photon energy approaches the semiconductor bandgap E_g, it is expected that nanostructuring will yield the greatest improvement in Φ_{int} for photons with energy slightly above E_g.

For indirect bandgap semiconductors with long $\alpha(\lambda)^{-1}$ such as Si[9,10] and GaP[11] the relationship between 3D structure and carrier collection has been studied in VLS-grown nano/microwire systems[2,10] and nanostructures etched from single-crystal wafers using dry,[12] wet,[13−15] and electrochemical anodization processes.[16−18]

The correlation between 3D structure and photoelectrode performance in direct bandgap absorbers with short $\alpha(\lambda)^{-1}$, such as GaAs, has not been well explored. GaAs and related III−V compounds are important solar materials due to high mobilities (μ), high $\alpha(\lambda)$, and compositionally tunable bandgaps.[19] GaAs is of particular interest because of the demonstration of world-record single-junction PV devices with 1-sun η = 28.8%,[20] as well as the ability to deposit solar-quality GaAs thin films by plausibly inexpensive and scalable vapor transport techniques.[21−24] Parkinson and coworkers showed that the photocurrent obtained from n-GaAs electrodes can be enhanced through a "matte" etch using a H_2SO_4/H_2O_2 solution. The increased photocurrent was attributed to reduced R.[13] However, reinspection of the published scanning electron microscope (SEM) images shows random roughening on the ~0.5 μm length scale which suggests that 3D carrier collection also likely contributed to improved carrier collection. Electrochemical anodization has also been shown to create nanoporous GaAs structures with a variety of pore geometries,[25−28] but the influence of the nanostructure on the photoelectrode performance has not been explored. Recently MOCVD-grown epitaxial GaAs and other III−V nanowire/nanopillar array solar devices have been reported.[29−32] However, the variable surface and bulk properties of these materials make it challenging to separate the influences of R, bulk recombination, and surface defects on the measured photoresponse.

Herein we report a combined PEC and optical R study of nanostructured n-GaAs photoelectrodes created using electrochemical anodization. The surface nanostructure depth and coverage was controlled by adjusting the anodization current density (J_{anod}) and time (t) without using lithography.[25−28] Photoresponse was analyzed using a ferrocene/ferrocenium electrolyte which makes a conformal rectifying contact to n-GaAs.[22,33,34] The R of the air/glass/solution/GaAs interface was directly measured using an integrating sphere. We used two n-GaAs wafers with different L_D to study how the nanostructure's influence on Φ_{int} changes with L_D. A two-step anodization procedure[25,26] was used to control pore depth and spacing, which allowed us to optimize surface nanostructure based on $\alpha(\lambda)$ and L_D. This study complements the previous work on anodized indirect bandgap semiconductors and demonstrates that rational nanostructuring can dramatically improve performance of photoelectrodes even when fabricated from materials with direct bandgaps and high $\alpha(\lambda)$.

RESULTS AND DISCUSSION

I. Anodization and Structure Characterization. The use of anodization to form pores in GaAs is well-known.[25,26,28] Application of an oxidizing potential to n-GaAs causes tunneling breakdown[35] of the space-charge layer,[26] providing holes at the semiconductor surface which subsequently oxidize the Ga and As and form species which are soluble in acidic or alkaline solution.[36] Using this technique both J_{anod} and the voltage applied during anodization (V_{app}) have been shown to influence the crystallographic orientation[28] and density[25] of pores.

In this study, pores were etched into the n-GaAs wafers by passing an anodic galvanostatic current density (J_{anod}) through the 1 M H_2SO_4 electrolyte as shown in Figure 2. On the basis of the Pourbaix diagrams,[36] the anodization of GaAs in 1 M H_2SO_4 at potentials greater than ~0.5 V vs NHE is expected to yield aqueous Ga^{3+} and H_3AsO_4. We used a two-electrode anodization cell with the Pt counter electrode evolving H_2. Because Pt is a good catalyst for H_2 evolution, the counter electrode potential is maintained near NHE. Given the observed range of V_{app} (1.8−5.4 V), the GaAs working electrode was undoubtedly positive of 0.5 V vs NHE. The anodic etching and

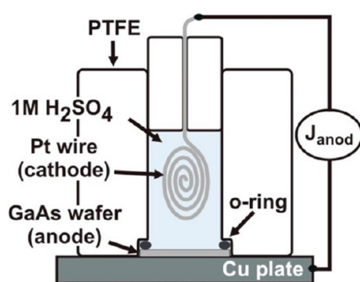
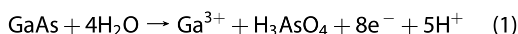
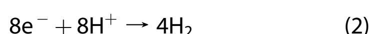


Figure 2. Schematic of the anodization cell used to fabricate nanostructured GaAs.

cathodic counter electrode reactions are thus given by eqs 1 and 2, respectively.



$$GaAs + 4H_2O \rightarrow Ga^{3+} + H_3AsO_4 + 8e^- + 5H^+ \quad (1)$$



$$8e^- + 8H^+ \rightarrow 4H_2 \quad (2)$$

Anodization parameters facilitated control of both the etch rate (which depends on J_{anod}) and the volume of material etched (v). As shown in eq 3, v depends on the charge passed per unit area, $Q = J_{anod} \cdot t$.

$$v = \frac{QMA}{n_e q N_A \rho} \quad (3)$$

where t is the etch duration, M is the molecular weight of GaAs, n_e is the number of moles of electrons per mole of GaAs oxidized, q is the fundamental charge, N_A is Avogadro's number, A is the area being anodized, and ρ is the density of GaAs.

Two wafers with different L_D (Si-doped GaAs with L_D = 170 nm and Te-doped GaAs with L_D = 420 nm) were used to investigate the relationship between nanostructure, Φ_{int}, and L_D. To study the effect of the etch rate on nanostructure, we adjusted J_{anod} and t (and measured V_{app}) while keeping Q constant at 1.4 C cm^{-2} (Table 1). From SEM analysis we find that as J_{anod} increased, the pore depth decreased (Figures 3 and 4). We note that samples prepared with $J_{anod} \leq 100$ mA cm^{-2} retained some planar areas on the surface. It has previously been shown that after a surface is covered with features to nucleate pores (such as etch pits[25] or surface texture[28]) a high pore density can be achieved by anodization. We thus also used a two-step anodization to fabricate samples having different pore depths while maintaining complete surface nanostructure coverage. The two-step anodization consisted of a brief pore nucleation step used to form a high density of shallow pores (J_{anod} = 150 mA cm^{-2} and t = 3 s) followed by a separate pore growth step used to deepen the existing pores (J_{anod} = 50 mA cm^{-2} and 20 s $\leq t \leq$ 76 s) for which t was varied to change Q (Table 1).[26] Throughout the text we refer to GaAs samples by the n-type dopant present in the wafer (Si or Te) and the relevant anodization parameter, that is, the value of J_{anod} (in mA cm^{-2}) for samples anodized using one step, or the value of Q (in C cm^{-2}) for samples anodized using two steps (Table 1).

TABLE 1. Anodization Parameters Used to Fabricate Nanostructured GaAs

sample name	L_D (nm)	planar, 1-step, or 2-step etch	J_{anod} (mA cm^{-2})	V_{app} (V)	t (s)	Q (C cm^{-2})	avg pore depth (μm)
Si-0	170	planar					
Si-25	170	1-step	25	1.8	56	1.4	1.7
Si-50	170	1-step	50	2.0	28	1.4	1.2
Si-100	170	1-step	100	2.6	14	1.4	0.6
Si-150	170	1-step	150	3.6	9.4	1.4	0.5
Si-200	170	1-step	200	4.4	7	1.4	0.3
Si-250	170	1-step	250	5.4	5.6	1.4	0.2
Te-0	420	planar					
Te-50	420	1-step	50	2.6	28	1.4	4.0
Te-150	420	1-step	150	3.5	9.4	1.4	1.5
Te-1.4	420	2-step	150/50	3.5/2.5	3/20	1.4	3.2
Te-2.8	420	2-step	150/50	3.5/2.5	3/47	2.8	3.9
Te-4.2	420	2-step	150/50	3.5/2.5	3/74	4.2	5.6

SEM analysis revealed that pores nucleated randomly across the surface but grew preferentially in the [111]B direction as has been previously observed by Föll and co-workers.[27] Figure 3 shows that the etching is more uniform and isotropic with a larger number of pores for increased J_{anod}. The etched nanostructures give rise to sub-λ trigonal prismatic features, which are expected to reduce R. The nanostructure depths of 0.2−5.6 μm are appropriate for studying lateral carrier collection based on the high $\alpha(\lambda)$ of GaAs.[37] These data suggest that anodization can be used to tailor n-GaAs nanostructures for solar devices, as we show below.

II. Photoelectrochemical Current−Potential Analysis. An electrolyte of ferrocene/ferrocenium in acetonitrile was used to provide conformal rectifying contacts to the n-GaAs photoelectrode (see Methods).[22,33,34] Current−potential (J−E) measurements were carried out under 100 mW cm^{-2} of AM1.5G solar simulation (1-sun) with rapid stirring to increase solution mass transport. All anodized samples showed improved short-circuit photocurrent (J_{SC}) relative to the planar n-GaAs controls (Figure 5). For anodized photoelectrodes Si-150 and Te-1.4, J_{SC} was improved by 250% and 195%, respectively, compared to planar controls made from the same wafers (Si-0 and Te-0).

The measured fill factor (ff) provides further insight into the operation of the nanostructured n-GaAs photoelectrodes. Unlike PV devices, the ff of PEC devices is affected by a voltage loss associated with the concentration overpotential (η_{conc}) required to drive the diffusion of redox species from the bulk solution to the photoelectrode surface.[38] η_{conc} increases for the anodized samples relative to planar controls because the photocurrent is higher. Correcting for η_{conc} (see SI) results in ff between 0.6 and 0.7 for all anodized samples, independent of J_{anod} and similar to the planar controls (Figure 5C,D). This indicates that the ff in the uncorrected J−E data is affected by mass

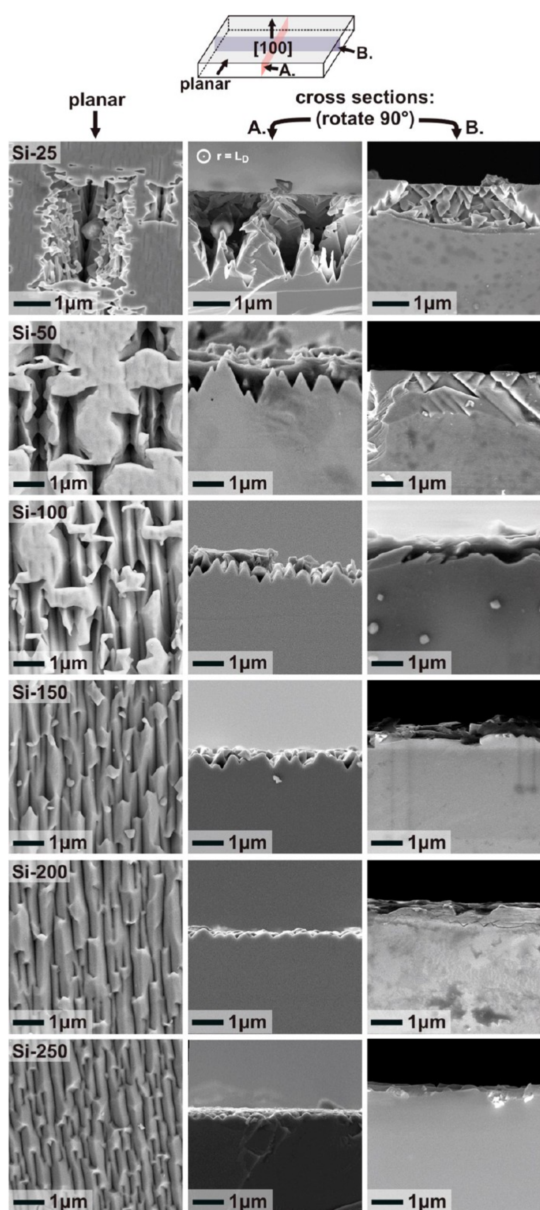


Figure 3. SEM micrographs of the anodized Si-doped (L_D = 170 nm) *n*-GaAs wafer viewed top-down (left column), in cross-section perpendicular to the long dimension of the pores (middle column), and in cross-section parallel to the long dimension of the pores (right column). The faces exposed in the two cross sections belong to the {110} of family of planes.

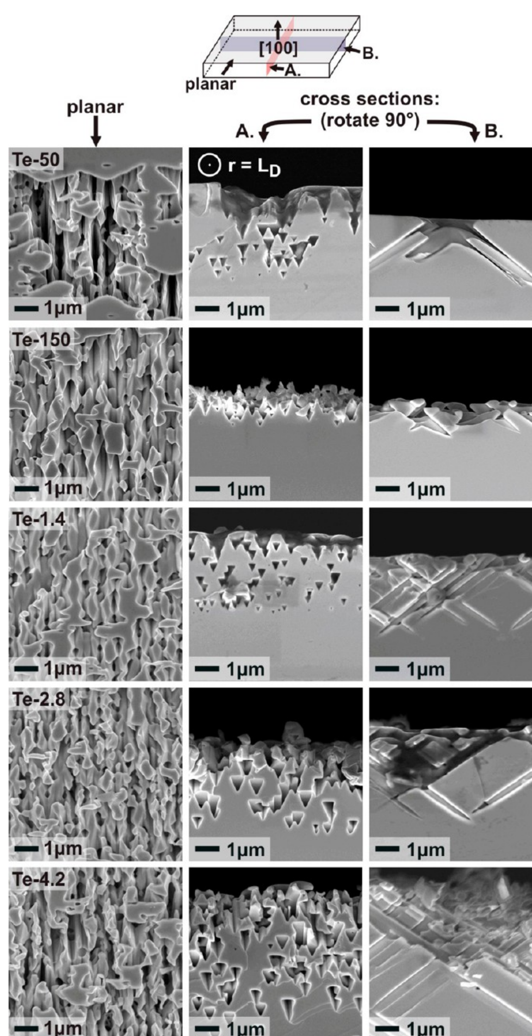


Figure 4. SEM micrographs of the anodized Te-doped (L_D = 420 nm) *n*-GaAs wafer viewed top-down (left column), in cross-section perpendicular to the long dimension of the pores (middle column), and in cross-section parallel to the long dimension of the pores (right column). The faces exposed in the two cross sections belong to the {110} of family of planes.

transport and series resistance losses inherent to the PEC technique and is not due to degradation of the anodized *n*-GaAs relative to the planar controls. The series resistance and overpotential losses can be reduced by either using higher concentrations of redox couple and supporting electrolyte, or by using thin-layer electrolyte geometries.[39]

III. Optical Reflectance as a Function of Nanostructure. The *R* of each photoelectrode surface was measured to determine how much of the increases in J_{SC} can be attributed to changes in *R*. To measure *R*, we used an integrating sphere with a custom holder that incorporates GaAs, acetonitrile, and a glass slide to duplicate the interfaces present in the PEC cell (i.e., air/glass/acetonitrile/GaAs).

All anodized samples had lower *R* than the planar controls (Figure 6). Although increases in J_{SC} correlate with decreased *R*, the change in *R* by itself does not account for the amount of increase in J_{SC}. The *R* of the air/glass/acetonitrile/GaAs interface for planar controls is approximately 0.27. J_{SC} for anodized samples increased up to 250% relative to planar controls (Figure 3). Thus, the enhanced J_{SC} for anodized samples relative to planar samples is due to decreased bulk recombination (resulting from 3D carrier collection) in addition to the decreased *R*.

At normal incidence, *R* is expected to be independent of sample orientation. However, because the sample holder in the integrating sphere is 8° off-axis (Figure 6B inset), *R* for the anodized GaAs was found to

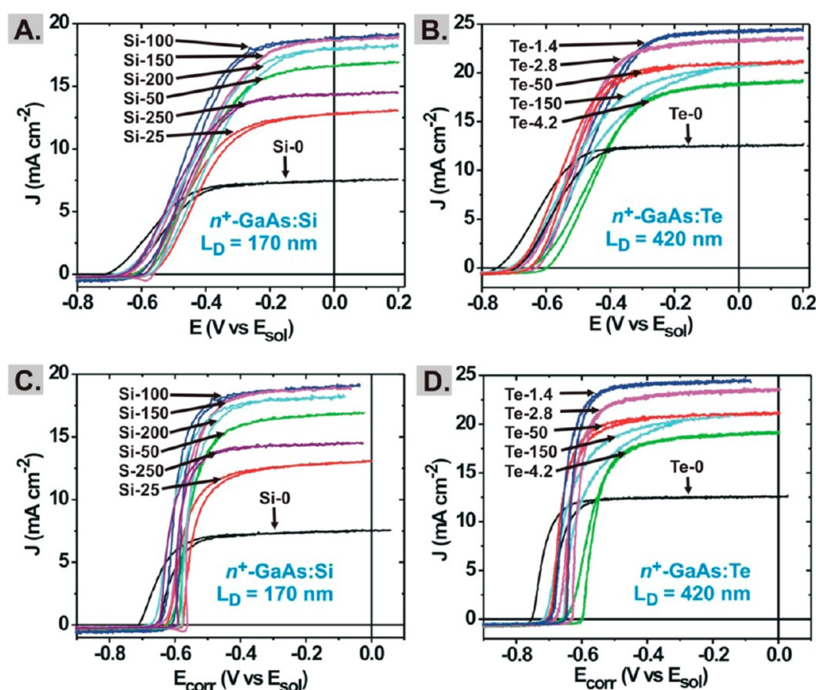


Figure 5. J–E curves of (A) anodized n-GaAs:Si (L_D = 170 nm) and (B) anodized n-GaAs:Te (L_D = 420 nm). The same data corrected for series resistance and concentration overpotential is shown in panels C and D.

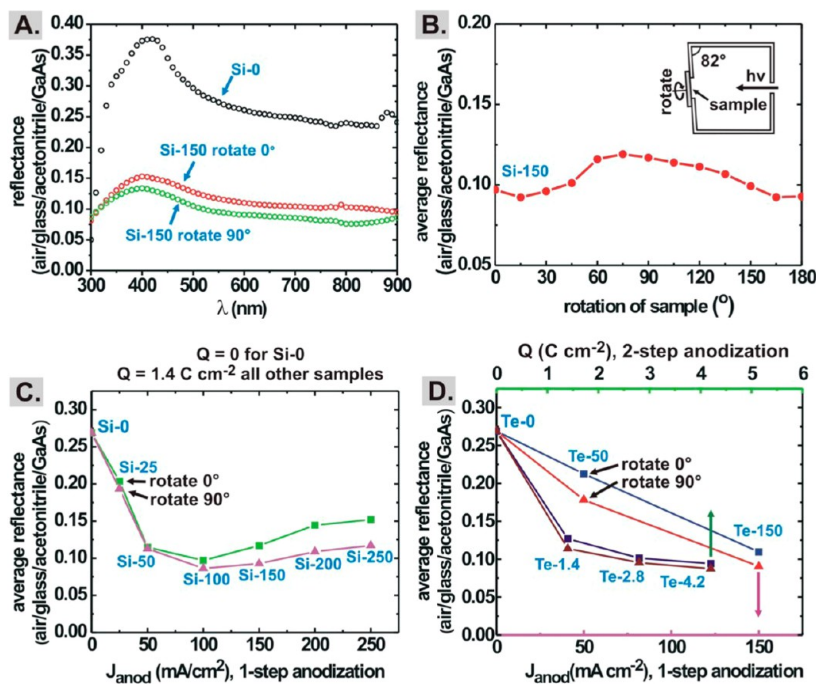


Figure 6. Measured R of the air/glass/acetonitrile/GaAs interface for all samples. (A) Reflectance of a planar GaAs control and sample Si-150 rotated 0 and 90°. (B) Average reflectance (300 nm < λ < 900 nm) of sample Si-150 measured as a function of rotation of the (100) surface. The inset depicts the sample position in the integrating sphere. (C,D) Average reflectance over λ = 300–900 nm for planar and anodized samples demonstrating the effects of J_{anod}, Q, and rotation on R. For 6D, the bottom axis is for samples anodized with 1 step (Te-50 and Te-150) and the top axis is for samples anodized with 2 steps (Te-1.4, Te-2.8, and Te-4.2).

vary when the samples were rotated around the ⟨100⟩ direction (Figure 6). The etched nanostructures are anisotropic with respect to rotation of the (100) plane (Figure 3 and 4) which results in the observed rotational dependence of R. The normal incidence R (for the purpose of calculating Φ_{int}) was approximated by averaging the R measured at 0° and 90° rotation (Figure 6B inset). The error in this approximation is small and of the same order as the error resulting from slight deviations from normal incidence encountered

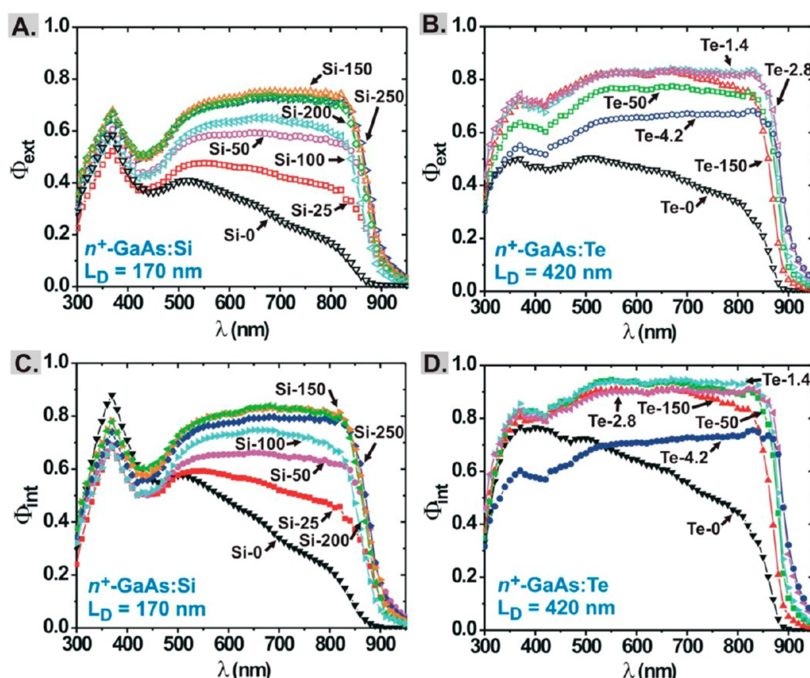


Figure 7. External quantum efficiency Φ_{ext} for *n*-GaAs with (A) L_D = 170 nm and (B) L_D = 420 nm. Internal quantum efficiency Φ_{int} for *n*-GaAs with (C) L_D = 170 nm and (D) L_D = 420 nm.

when making the physical electrodes, clamping the PEC cell in place, and positioning the solar simulator, and was therefore neglected.

The R of samples decreased with increasing J_{anod} until a minimum was reached at J_{anod} = 100 mA cm^{-2}, and then R increased up to J_{anod} = 250 mA cm^{-2} (Figure 6C). For samples Te-1.4, Te-2.8, and Te-4.2, which were etched using the two-step process, we observed a slight decrease in R as Q was increased (Figure 6D). The trends in R are consistent with analysis of the SEM images. The surfaces of the lowest R samples consist of v-shaped pores that are approximately 0.5 μm deep with sub-λ lateral dimensions. The highest R samples all possessed either pores shallower than λ or unetched flat regions (see Figures 3 and 4), both of which present an abrupt change in n for incident photons and thus increased R at the semiconductor/solution interface relative to the optimally etched samples.

IV. Minority Carrier Collection. To understand the influence of nanostructure on the collection of photogenerated minority carriers, we measured the external quantum efficiency (Φ_{ext}) (Figure 7A,B) and corrected it for R to obtain the internal quantum efficiency (Φ_{int}):

$$\Phi_{int} = \frac{\Phi_{ext}}{1 - R} \quad (4)$$

If changes in J_{SC} were solely due to decreased R of the anodized GaAs, Φ_{int} would be identical for all samples. However, the Φ_{int} of anodized samples is higher than the Φ_{int} of planar controls. Thus increased J_{SC} for the anodized samples is due not only to reduced R, but also due to an improved collection of minority carriers, particularly of those generated by photons with energy slightly above E_g (Figure 7C,D). The combination of the enhanced optical in-coupling and carrier-collection results in significantly increased Φ_{ext} for the anodized samples relative to the planar controls Si-0 and Te-0. Over the range of nanostructures explored, the relative improvement from control to anodized samples was greatest for Si-doped GaAs with L_D = 170 nm. The Φ_{ext} was highest, however, for the optimally anodized Te-1.4 which had a longer L_D = 420 nm.

V. Overall Photoelectrode Structure–Performance Trends. Observed trends in R, Φ_{ext}, and J_{SC} are plotted as a function of the anodization variables J_{anod} and Q in Figure 8. The observed trends in R are consistent with enhanced optical in-coupling due to the v-shaped sub-λ nanostructures observed *via* SEM. The trends in Φ_{ext} are the result of enhanced light absorption and decreased bulk recombination due to 3D carrier collection.

To check the consistency of the quantum efficiency and J–E data, Φ_{ext} was used to calculate the expected J_{SC} under 1-sun illumination ($J_{SC,calc}$) by integrating the product of the solar flux and Φ_{ext}. Trends in $J_{SC,calc}$, J_{SC}, wavelength averaged normal-incidence R in air, and wavelength average normal-incidence R of the air/glass/acetonitrile/GaAs interface are compared in Figure 8. The values of $J_{SC,calc}$ are 2–3 mA cm^{-2} higher than the values of J_{SC} measured under 1-sun illumination. This discrepancy is due to light absorption by the concentrated electrolyte used in the 1-sun measurements,

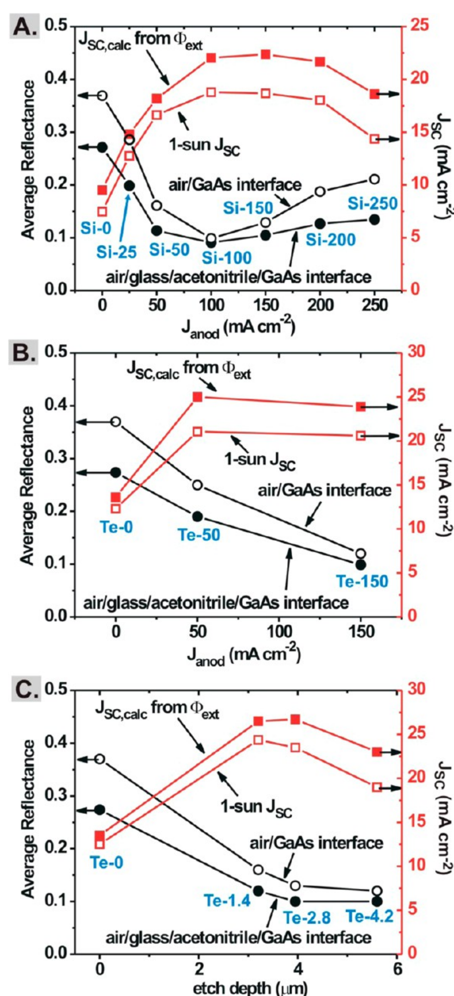


Figure 8. Trends in photoelectrode response as a function of anodization parameters. On each panel is plotted J_{SC} calculated from Φ_{ext} measurements, J_{SC} under AM1.5G solar simulation, average R in air, and average R of the air/glass/acetonitrile/GaAs interface: (A) samples Si-0 through Si-250 (one-step anodization); (B) samples Te-0 through Te-150 (one-step anodization); (C) samples Te-0 through Te-4.2 (two-step anodization).

which was required to sustain the mA-range photocurrent. In contrast, Φ_{ext} was determined from nA-range photocurrent measurements, which made it possible to reduce the concentration of the light-absorbing electrolyte by diluting it 1:10 with dry acetonitrile. Remeasuring Φ_{ext} in undiluted electrolyte yielded values of $J_{SC,calc}$ within ±0.5 mA of the observed J_{SC} (Supporting Information, Figure S3A). Therefore, the 1-sun J_{SC} attainable in optimized cells without parasitic electrolyte absorption is expected to be 2−3 mA higher than what was measured here.

Besides Φ_{ext} and ff, the photovoltage is an important performance metric. At constant light flux, the ideal diode equation predicts that the photovoltage will decrease by 59 mV times the diode ideality factor n_{dio}, per order-of-magnitude increase in the charge-separating junction area, in this case the area of the electrode−electrolyte interface.[1,4] As expected, the anodized samples exhibited lower photovoltages than planar controls. On the basis of SEM cross sections, the roughness factors of the anodized Si-doped *n*-GaAs samples range from 1.3 (Si-25) to 2.5 (Si-150). On the basis of this increased junction area, the predicted decrease in photovoltage should be 7 mV to 25 mV multiplied by n_{dio}. The observed photovoltages decreased by 20 mV to 50 mV relative to the planar controls, suggesting $n_{dio} \approx 2$.

Sample Te-1.4 was etched *via* the two-step anodization and had the highest Φ_{int} measured, 0.94 at λ = 830 nm, despite having L_D = 420 nm, which is short relative to $\alpha(\lambda)^{-1}$. This represents a 2.8-fold Φ_{int} enhancement relative to the planar control Te-0. This near-ideal structure, which was introduced without lithography *via* potentially inexpensive and rapid anodization, had pores with almost an ideal spacing of ∼2 × L_D and depth greater than $\alpha(\lambda)^{-1}$ (Figure 1). Further increases to Φ_{ext} could be achieved by treating the glass/air surface ($R \approx 0.04$) with an antireflective coating. For comparison, Te-150 was etched with a one-step anodization and showed similar Φ_{int} to Te-1.4, except for λ between 800 and 900 nm where deeper pores in Te-1.4 provide 3D carrier collection pathways for weakly absorbed photons (photons having energy near E_g). Te-4.2, which had pores roughly twice as deep as Te-1.4, showed significantly lower Φ_{int} for all λ, which is inconsistent with the simple radial junction model.[4] Figure 4 shows that Te-4.2 also contained smaller near-surface features (*e.g.*, < 50 nm) than Te-1.4 after the longer etching process. Photogenerated minority carriers in such features smaller than the depletion width (here, ∼40 nm) may be subject to increased recombination.[9] The highest Φ_{int} for the Si-doped samples was ∼0.82. The Φ_{int} for the Si-doped samples is likely lower than for the Te-doped samples because the natural dimensions of the etched nanostructures are larger than 2 × L_D, and because of increased depletion-region recombination (due to the lower L_D).

CONCLUSION

We have demonstrated the use of electrochemical anodization to introduce a controllable surface nanostructure in *n*-GaAs photoelectrodes. Preferential etching in the [111]B direction[26] gives rise to triangular prismatic pores which result in reduced R, as predicted by effective medium theory and discussed by others.[2,3] Internally consistent R, J−E, Φ_{int}, Φ_{ext}, and SEM analysis indicate that the high J_{anod} needed for low R interfaces is not suitable for making deep pores, as the surface is etched nearly as fast as the pore bottoms, possibly due to mass-transport limitations or a change in etching anisotropy.[28] Thus, moderate J_{anod} = 150 mA cm^{-2} led to effective optical in-coupling and low R but did not yield the highest Φ_{int} for GaAs with $L_D < \alpha(\lambda)^{-1}$. Low J_{anod} resulted in pores with controllable depth, but the

barrier for nucleation of new pores prevented uniform texturing of the planar surface and resulted in relatively high R. A two-step anodization consisting of a high J_{anod} pore nucleation step and a low J_{anod} pore growth step was used to circumvent this problem and found to be optimal.

The methods reported here could have impact in several areas. The performance of low-cost GaAs deposited on foils or other substrates[40−43] could be substantially improved by controllably anodizing to reduce R, introduce nanostructuring at a length-scale appropriate for the material quality, and reduce the influence of grain boundaries. The performance of GaAs photoelectrodes possessing $L_D > \alpha(\lambda)^{-1}$, such as those deposited by close-spaced vapor transport (CSVT),[22−24] could be improved by anodization at high-J_{anod} to introduce surface nanotexture optimized to minimize R. If applied as water-splitting photoelectrodes (after protection of the GaAs surface and incorporation of an electrocatalyst),[44] the decrease in photovoltage caused by increased junction area is expected to be compensated by the reduction of kinetic overpotential due to increased catalyst surface area.[1]

METHODS

Sample Preparation. Ohmic back contacts (50 nm evaporated AuGe eutectic diffused at 450 °C for 90 s in 5% H_2 95% N_2) were made to commercial ⟨100⟩-oriented vertical-gradient-freeze (VGF) grown n-GaAs wafers with different L_D. One wafer was doped n-type with Si (L_D = 170 nm, $N_D = 3 \times 10^{18}$ cm^{-3}) and the other was doped with Te (L_D = 420 nm, $N_D = 7 \times 10^{18}$ cm^{-3}). The samples were sealed in a custom PTFE cell (Figure 2) containing 1 M sulfuric acid. The cell made a seal to the wafer surface with a compressed O-ring (inner area of 0.54 cm^2). Galvanostatic experiments were performed in two-electrode mode using a Biologic SP-200 potentiostat.

***J*−*E* Characterization.** Photoelectrodes utilizing planar and anodized n-GaAs were constructed using standard methods.[22] AuGe ohmic back contacts were attached to tinned-copper wires using silver paint and the wires were fed through glass tubes. The GaAs wafers were bonded to the wire/glass assembly and an active device area of ∼0.03 cm^2 was defined with nonconductive epoxy (Loctite Hysol 9460). Electrode areas were individually measured with a digital scanner and ImageJ software. For $J-E$ measurements, electrodes were immersed in an electrolyte containing 100 mM sublimed ferrocene, 0.5 mM recrystallized ferrocenium, and 1 M $LiClO_4$ (Alfa Aesar, 99%) in dry acetonitrile. All samples and controls were dipped in aq 1 M HCl, rinsed with 18.2 MΩ water, and blown dry with N_2, immediately before all PEC and spectral response measurements to remove the native oxide.[45] $J-E$ measurements were conducted in three-electrode mode under 100 mW cm^{-2} of AM1.5G solar simulation (Abet Technologies 10500). $J-E$ curves were recorded at a scan rate of 20 mV s^{-1}. The counter electrode was Pt mesh and the reference electrode was a Pt wire poised at the solution potential positioned ∼1 mm from the working electrode to minimize uncompensated series resistance. Hysteresis in the forward and backward $J-E$ curves is likely related to chemical differences of the GaAs surface (*e.g.*, surface charge) after the anodic and cathodic portions of the potential sweep. Hysteresis is typical for GaAs PEC measurements.[33,34,46]

Reflectance Characterization. The R of anodized GaAs samples was measured in an integrating sphere. We measured the air/GaAs interface, and the air/glass/acetonitrile/GaAs interface which is relevant to the PEC measurements (which were conducted in a glass cell containing acetonitrile). The R of the air/glass/acetonitrile/GaAs interface was measured by placing a drop of acetonitrile between the etched GaAs surface and a glass slide and loading the assembly onto the integrating sphere.

SEM Characterization. The nanostructure of the anodized n-GaAs samples was characterized using a Zeiss Ultra-55 SEM with in-lens detector. Cross sections were prepared by cleaving the etched wafers and mounting the cleaved surfaces vertically in the SEM holder. The working distance was ∼5 mm, and an accelerating voltage of 5 kV was used.

Spectral Response Determination of Φ_{ext}, Φ_{int}, and L_D. Spectral response was measured at short-circuit (0 V *vs* Pt) using the electrolyte described above diluted by a factor of 1:10 with dry acetonitrile as discussed in section V and in the Supporting Information (Figure S3). The monochromatic light was chopped at 35 Hz and the nA-range signal was measured using a lock-in amplifier (Bentham PVE300). The chopped signal from samples and controls produced a signal free of transients with amplitude independent of chopping frequency in the range studied (Supporting Information, Figure S4). The light intensity was measured using a calibrated Si reference photodiode (Bentham Si-11677) to determine Φ_{ext}. The Φ_{int} was calculated according to eq 5, where R is the normal-incidence R of the air/glass/acetonitrile/GaAs interface as discussed in section III. The calculation of Φ_{int} did not compensate for solution absorbance.

The values of L_D reported throughout were determined by fitting Φ_{int} of the planar wafers (Supporting Information, Figure S3) to the Gärtner model of carrier collection eq 5 over the region from 550 to 870 nm which is nearly unaffected by solution absorbance.

$$\Phi_{int} = \left(1 - \frac{e^{-\alpha(\lambda)W}}{1 + \alpha(\lambda)L_D}\right) \quad (5)$$

The Gärtner model assumes no recombination within the depletion width (W) and that recombination in the quasi-neutral region is governed by L_D.[47,48] This technique yields values of L_D that are similar to those obtained by electron beam induced current measurements for n-GaAs.[49]

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: Expanded methods and discussion of nonaqueous PEC and galvanostatic anodization experiments. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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